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Date: December 2, 1999
Docket No.: 0465-0636P-SP

Assistant Commissioner for Patents
Box PATENT APPLICATION
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): YANG, Hae Chang

For: ESD PROTECTION CIRCUIT AND METHOD FOR FABRICATING THE SAME

Enclosed are:

X A specification consisting of 12 pages

X 5 sheet(s) of Formal drawings

X An assignment of the invention

X Certified copy of Priority Document(s)

X Executed Declaration X Original ___ Photocopy

___ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27

X Preliminary Amendment

X Information Disclosure Statement, PTO-1449 and reference(s)

___ Other _____

The filing fee has been calculated as shown below:

			LARGE ENTITY			SMALL ENTITY	
FOR	NO. FILED	NO. EXTRA	RATE	FEE		RATE	FEE
BASIC FEE	********** ********** **********	********** ********** **********	***** ***** *****	$760.00	or	**** **** ****	$380.00
TOTAL CLAIMS	5 - 20 =	0	x18 =	$ 0.00	or	x 9 =	$ 0.00
INDEPENDENT	3 - 3 =	0	x78 =	$ 0.00	or	x 39 =	$ 0.00
MULTIPLE DEPENDENT CLAIM PRESENTED	no		+260 =	$ 0.00	or	+130 =	$ 0.00
			TOTAL	$ 760.00		TOTAL	$ 0.00

X A check in the amount of $ 800.00 to cover the filing fee and recording fee (if applicable) is enclosed.

___ Please charge Deposit Account No. 02-2448 in the amount of $_____. A triplicate copy of this transmittal form is enclosed.

___ No fee is enclosed.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. 1.16 or under 37 C.F.R. 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____

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IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicants: YANG, Hae C.

Serial No.: New Group:

Filed: December 2, 1999 Examiner:

For: ESD PROTECTION CIRCUIT AND METHOD FOR FABRICATING THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

December 2, 1999

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE CLAIM:

SECOND CLAIM 2: Line 1, change "claim 2" to -Claim 3--

*** * * * REMARKS * * * ***

The amendment to the claim corrects an inadvertent typographical error to place the application into better form prior to examination.

Favorable action on the above-identified application is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-22448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, extension of time fees.

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ESD PROTECTION CIRCUIT AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an ESD(Electro-Static Discharge) protection circuit, and more particularly, to an ESD protection circuit and a method for fabricating the same, which has an improved performance.

Background of the Related Art

Fig. 1 illustrates a system of a related art ESD protection circuit. In general, a maximum field strength against which an oxide film in an MOS transistor can endure is 6MV/cm, which corresponds to 30V if the oxide film is scaled up to a thickness of 50nm. A voltage of this range can be generated from a minute static electricity occurred around a circuit with easy. There is ceaseless generation of static electricity when a human body makes movement, and the human body acts as a carrier that carries a great amount of charge. Therefore, if the human body comes closer to a conductor, the static electricity is discharged, causing a great current to flow within a short time. Thus, as an amount of charge that can break the transistor is very small, an ESD protection circuit 2 is provided to an input pin between a pad 1 and a main chip 3 so that the static electricity, rushing into an inner part of the main chip 3, is discharged through an appropriate circuit for maintaining voltages on an input terminal and an output terminal within fixed ranges. Thus, an input protection circuit and an output protection circuit are required for prevention of static breakdown.

A related art ESD protection circuit will be explained with reference to the attached drawings. Fig. 2 illustrates a first exemplary related art ESD protection circuit, and Fig. 3 illustrates a second exemplary related art ESD protection circuit.

Referring to Fig. 2, the first exemplary related art ESD protection circuit is provided with

a plurality of first transistors 11 each having a collector connected to an input pin between a pad 1 and a main chip 3, and a gate and an emitter both grounded, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of a static electricity is bypassed to the first transistors 11, thereby protecting the main chip 3.

Referring to Fig. 2, the second exemplary related art ESD protection circuit is provided with a plurality of second transistors 12 each having a collector connected to an input pin between a pad 1 and a main chip 3 through a first resistor 21, a gate grounded, and an emitter grounded through a second resistor 22, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of a static electricity is bypassed to the second transistors 12, thereby protecting the main chip 3.

However, the related art ESD protection circuits and methods for fabricating the same have the following problems.

First, the related art ESD protection circuit, having the plurality of first transistors each with the collector connected to the input pin between the pad and the main chip and the gate and the emitter both grounded, i.e., no resistor is connected to the emitter/collector, may be involved in occurrence of breakage of a particular point caused by momentary concentration of a charge on the particular point in a case of a BJT of a single or plural units or in a case the static electricity is occurred from inside, and a space of the ESD protection circuit for preventing such a occurrence requires a larger area.

Second, the related art ESD protection circuit, having the plurality of the second transistors each with the collector connected to the input pin between the pad and the main chip through the first resistor, the gate grounded, and the emitter grounded through the second resistor, is involved in a reduction of a BJT gain caused by the two resistors connected to the emitter

/collector and a drop of an ESD capability.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an ESD protection circuit and a method for fabricating the same that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an ESD protection circuit and a method for fabricating the same, which has an improved performance.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the ESD protection circuit includes a substrate, a transistor formed on the substrate, a first insulating film formed on the substrate inclusive of the transistor and having a first contact hole to an input terminal of transistor, a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor, a second insulating film formed on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer, and a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer.

In another aspect of the present invention, there is provided a method for fabricating an ESD protection circuit, including the steps of (1) forming a transistor on a substrate, (2) forming

a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor, (3) forming a buffered layer in the first contact hole and the first insulating film in the vicinity of the first contact hole, (4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer, and (5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention:

In the drawings:

Fig. 1 illustrates a system of a related art ESD protection circuit;

Fig. 2 illustrates a first exemplary related art ESD protection circuit;

Fig. 3 illustrates a second exemplary related art ESD protection circuit;

Fig. 4 illustrates an ESD protection circuit in accordance with a preferred embodiment of the present invention;

Fig. 5 illustrates a section of an ESD protection circuit in accordance with a preferred embodiment of the present invention; and,

Figs. 6a ~ 6c illustrates sections showing the steps of a method for fabricating an ESD

protection circuit in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Fig. 4 illustrates an ESD protection circuit in accordance with a preferred embodiment of the present invention, Fig. 5 illustrates a section of an ESD protection circuit in accordance with a preferred embodiment of the present invention, and Figs. 6a ~ 6c illustrates sections showing the steps of a method for fabricating an ESD protection circuit in accordance with a preferred embodiment of the present invention.

Referring to Fig. 4, the ESD protection circuit in accordance with a preferred embodiment of the present invention includes a plurality of transistors 31 each having a collector connected to an input pin between a pad 1 and a main chip 3 through a resistor 32 and a gate and a emitter both grounded, wherein a voltage from the pad 1 is provided to the main chip 3 directly in a regular case and an inflow of a static electricity is bypassed to the second transistors 31, thereby protecting the main chip 3.

The ESD protection circuit of the present invention may be fabricated utilizing an NMOS transistor fabricating method, to have the following structure.

Referring to Fig. 5, the ESD protection circuit of the present invention includes an NMOS transistor 42 formed on a semiconductor substrate 41, a first ILD(InterLayer Dielectric) layer 43 formed on the semiconductor substrate 41 inclusive of the NMOS transistor 42 and having a first contact hole to a drain of the NMOS transistor 42, a buffered layer 44 formed on the ILD layer 43 inclusive of the first contact hole and electrically connected to the drain for acting as a resistor, a second ILD layer 43 formed on the first ILD layer 43 inclusive of the buffered layer

44 and having a second contact hole to the buffered layer 44, and a pad 1 formed on the second ILD layer 45 inclusive of the second contact hole and electrically connected to the buffered layer 44, for discharging a static electricity through the pad 1, the buffered layer 44, the drain of the NMOS transistor 42, and the source of the NMOS transistor 42.

A method for fabricating an ESD protection circuit in accordance with a preferred embodiment of the present invention will be explained with reference to Figs. 6a ~ 6c.

Referring to Fig. 6a, the method for fabricating an ESD protection circuit in accordance with a preferred embodiment of the present invention starts with forming an NMOS transistor 42 on a semiconductor substrate 41. As shown in Fig. 6b, a first ILD layer 42 and a first photoresist film are formed on the semiconductor substrate 41 inclusive of the NMOS transistor 42, and subjected to selective exposure and development to remove only a portion of the first photoresist film in which a first contact hole to a drain of the NMOS transistor 42 is to be formed. The selectively exposed and developed first photoresist film is used as a mask in etching the first ILD layer selectively, to form a first contact hole, and, then, the first photoresist film is removed. Polysilicon and a second photoresist film are formed on the first ILD layer 43 inclusive of the first contact hole, and the second photoresist film is subjected to selective exposure and development to leave the second photoresist film only on a region on which a buffered layer is to be formed. In this instance, instead of the polysilicon, a silicide may be used. The selectively exposed and developed second photoresist film is used as a mask in etching the polysilicon selectively, to form a buffered layer 44, and, then, the second photoresist film is removed. As shown in Fig. 6c, a second ILD layer 45 and a third photoresist film are formed on the first ILD layer 43 inclusive of the buffered layer 44, and the third photoresist film is subjected to selective exposure and development to remove a portion of the third photoresist film in which a second

contact hole to the buffered layer 44 is to be formed. The selectively exposed and developed third photoresist film is used as a mask in selective etching of the second ILD layer 45, to form a second contact hole, and, then, the third photoresist film is removed. Then, a pad 1 is formed on the second ILD layer 45 inclusive of the second contact hole.

Because the ESD protection circuit of the present invention has a plurality of transistors each with a collector only connected to an input terminal through a resistor, connected to an input pin between a pad and a main chip, and a gate and an emitter both grounded, the ESD protection circuit and the method for fabricating the same is favorable for use in a fast speed device which should have a small input capacitor, because the resistor at the input terminal increases a secondary breakdown voltage and distributes an static electricity so as not to concentrate on a particular point, the particular point breakage can be prevented, and because the ESD protection circuit of the present invention has a BJT gain greater than the related art ESD protection circuit having resistors connected both to the emitter/the collector, an ESD protection capability is improved.

It will be apparent to those skilled in the art that various modifications and variations can be made in the ESD protection circuit and the method for fabricating the same of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is Claimed is:

1. An ESD(Electro-Static Discharge) protection circuit comprising:

a pad and a maim chip; and,

a plurality of transistors each connected between the pad and the main chip and having a resistor connected only to an input terminal.

2. An ESD protection circuit comprising:

a substrate;

a transistor formed on the substrate;

a first insulating film formed on the substrate inclusive of the transistor and having a first contact hole to an input terminal of transistor;

a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor;

a second insulating film formed on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer.

2. A method for fabricating an ESD protection circuit, comprising the steps of:

(1) forming a transistor on a substrate;

(2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor;

(3) forming a buffered layer in the first contact hole and the first insulating film in the

vicinity of the first contact hole;

(4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

(5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole.

4. A method as claimed in claim 3, wherein the buffered layer is formed of polysilicon.

5. A method as claimed in claim 3, wherein the buffered layer is formed of a silicide.

ABSTRACT

ESD protection circuit and method for fabricating the same, which has an improved performance, the method including the steps of (1) forming a transistor on a substrate, (2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor, (3) forming a buffered layer in the first contact hole and the first insulating film in the vicinity of the first contact hole, (4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer, and (5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole.

FIG.1
Related Art

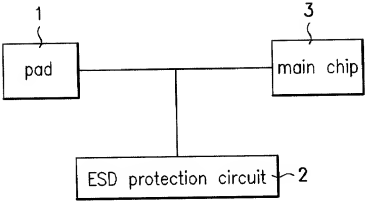


FIG.2
Related Art

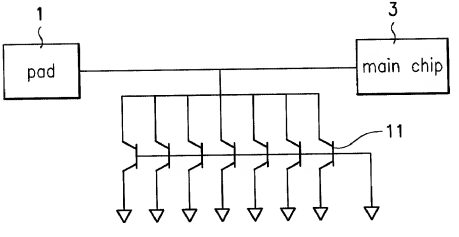


FIG.3
Related Art

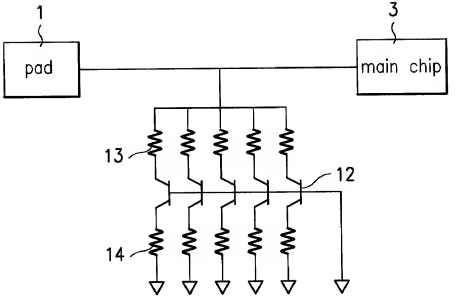


FIG.4

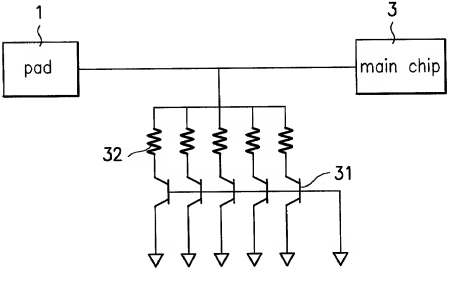


FIG.5

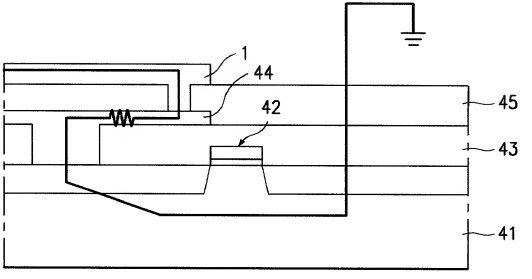


FIG.6A

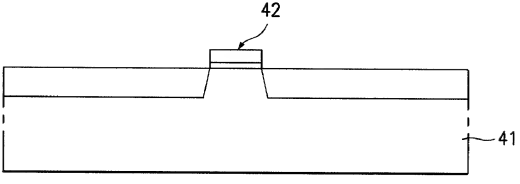


FIG.6B

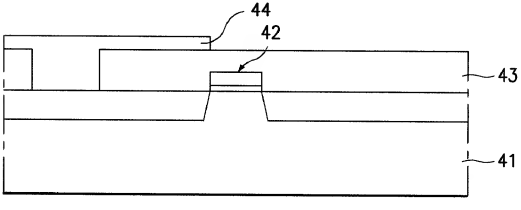
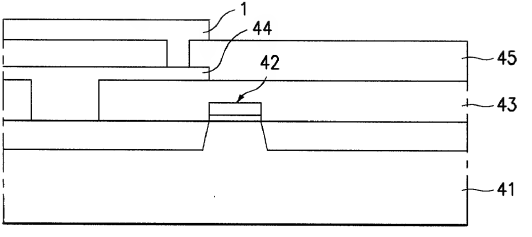


FIG.6C



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COMBINED DECLARATION AND POWER OF ATTORNEY

FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO.
465-636P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title:

ESD PROTECTION CIRCUIT AND METHOD FOR FABRICATING THE SAME

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____; and /or

the specification was filed on _____ as PCT
International Application Number _____; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)

Prior Foreign Application(s)			Priority Claimed
9231/1999 (Number)	Korea (Country)	March 18, 1999 (Month/Day/Year Filed)	XX Yes ☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No

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Insert Provisional Application(s): (if any)

(Application Number) (Filing Date)

(Application Number) (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

Insert Requested Information: (if appropriate)

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S. Application(s): (if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor:
Insert Name of Inventor
Insert Date This Document is Signed

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GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE*

Residence (City, State & Country) | CITIZENSHIP

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

* DATE OF SIGNATURE